

NREL/TP--214-4481

DE92 001153

Research on Advanced Photovoltaic Manufacturing Technology

Final Subcontract Report 1 March 1991 - 4 June 1991

T. Jester, C. Eberspacher
Siemens Solar Industries
Camarillo, California

NREL technical monitor: R. Mitchell



National Renewable Energy Laboratory
(formerly the Solar Energy Research Institute)
1617 Cole Boulevard
Golden, Colorado 80401-3393
A Division of Midwest Research Institute
Operated for the U.S. Department of Energy
under Contract No. DE-AC02-83CH10093

Prepared under Subcontract No. XC-1-10057-4

November 1991

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Printed in the United States of America
Available from:
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

Price: Microfiche A01
Printed Copy A03

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I. EXECUTIVE SUMMARY

This report outlines opportunities for significantly advancing the scale and economy of high-volume manufacturing of high-efficiency photovoltaic (PV) modules. We propose to pursue a concurrent effort to advance existing crystalline silicon module manufacturing technology and to implement thin film CuInSe_2 (CIS) module manufacturing. This combination of commercial-scale manufacturing of high-efficiency crystalline silicon modules and of pilot-scale manufacturing of low-cost thin film CIS technology will support continued, rapid growth of the U.S. PV industry.

The proposal for advancing crystalline silicon technology addresses expanding U.S. commercial production capacity, increasing module performance, and decreasing module manufacturing costs. The primary opportunities identified for expanding U.S. manufacturing capacity are the improvement of single crystal ingot yields and growth rates, and the development of thin wafer sawing and thin cell processing technologies. The primary opportunities identified for increasing module performance are improvements in silicon crystal quality, in impurity gettering and junction diffusion processes, in electrical contacting techniques, and in antireflection coatings and surface passivation processes. The primary opportunities identified for decreasing module manufacturing costs are cell processing and module assembly automation, module design and materials improvements, and manufacturing waste reductions.

The proposal for implementing thin film CIS module manufacturing focuses on establishing U.S. commercial production capacity and on realizing the low manufacturing costs possible with thin film processing. The primary requirements identified for establishing U.S. manufacturing capacity are the development of deposition and patterning processes suitable for high-volume production of large-area modules, and the integration of module processing, handling, and transport to minimize labor costs and maximize equipment productivity. The primary opportunities identified for realizing low manufacturing costs are fully automated substrate-to-module processing, high materials use efficiency, and a better understanding of the source materials specifications needed for high-efficiency module performance.

The implementation of the improvements identified in crystalline silicon module technology could halve PV module cost and could double SSI's U.S. manufacturing capacity. The implementation of the opportunities identified in thin film CIS module technology could create a new thin film PV technology with high-volume manufacturing costs substantially below those of any competing solar technology.

II. INTRODUCTION

The photovoltaic (PV) industry is at a critical stage of development at the start of the last decade of this millennium. During the previous decade, many of the basic assumptions that had formed the foundation of the original business planning by the PV companies were changed profoundly. The Photovoltaics Manufacturing Initiative (PVMaT) provides essential leverage to facilitate the U.S. PV industry seizing the opportunities created by these changes and solidifying its leading role in PV technology development and PV manufacturing output.

A. FOSSIL FUEL AVAILABILITY AND PRICE

A decade ago, crude oil prices were projected to climb rapidly and steadily to levels over \$50/barrel. Following the two "oil shocks" of the 1970's, even the assumption of a continuing, secure supply of fossil fuels was in question. Much of the early investment in PV was predicated on this scenario of high oil prices and/or limited availability. However, by the middle of the decade crude oil prices were again at very low levels, and oil appeared to be in substantial over-supply. Many of the oil companies that had been investing in the U.S. PV industry withdrew from the business during the 1980's. These divestment decisions were based in part on the expectation of long-term availability of crude oil at moderate prices.

Recent events in the Middle East, while once again emphasizing the volatile nature of world politics, have also shown a firm resolve on the part of both producers and consumers to keep oil prices from climbing to levels that would precipitate rapid radical changes within the existing fossil fuel based energy economy.

In stark contrast to a decade ago, today's PV industry is faced with widespread expectations of relatively stable longer term availability and pricing of fossil fuels.

B. ENVIRONMENTAL AWARENESS

Environmental awareness is creating an opposing trend to the relatively more secure outlook for long-term supply and price of conventional fuels. The assumptions of long-term use of fossil fuels are being challenged by recent concerns about global warming, acid rain, and other subsidiary effects of widespread hydrocarbon fuel combustion. The accident at the nuclear power plant in Chernobyl confirmed many of the public's latent fears concerning nuclear technology, and heightened the level of scrutiny that is now applied to issues of inherent reactor safety, disposal of radioactive waste products, and realizable costs.

This environmental, rather than economic, focus has generated debate about the future viability of conventional sources of energy. The debate has shifted from a moderately quantifiable analysis of fuel price and supply risks to generally more subjective and less quantifiable issues such as public health and societal morality.

The past decade has seen a broad acceptance of what was previously perceived as a narrow environmentalist sentiment. Perhaps more importantly, as public opinion is gradually but inexorably transformed into Government policy, economic incentives and/or penalties will likely become an increasingly significant mechanism in accelerating the penetration of alternate sources of energy into the broad generation mix.

In part due to this increasing environmental awareness, there is a much broader and more complex base of support for photovoltaic technology today than existed a decade ago.

C. PV MARKETS

The perceived character of the PV market has also undergone a substantial shift during the past decade. In the early 1980's, most PV systems were being installed to power remote industrial loads such as telecommunications repeaters, offshore aids to navigation, and cathodic protection systems. This strong industrial focus effectively set a product standard (30-50 watts, aluminum frames, tempered glass front, 12 volt nominal modules) that has endured until the present. A nascent market for electrification of remote homes constituted the only true non-industrial applications.

Superimposed on this small, conservative, existing market was a more distant vision of large scale implementation of PV in the utility grid as a substitute for traditional central generating facilities. This vision fueled much of the initial investment in the PV industry, and was consistent with the scenarios for rapidly escalating fossil fuel prices prevalent at the time.

In retrospect, three factors were primarily responsible for the lack of success in realizing this vision during the previous decade. First of all, as mentioned previously, oil price forecasts were dramatically revised. This reduced real economic pressure to pursue alternate energy sources, and de-emphasized the utility industry's interest in pursuing demonstration projects that might have led the PV industry down a iterative experiential system implementation cost reduction curve.

Secondly, PV technology as practiced in the early 1980's was not ready to be scaled up to high-volume capacity levels. Single crystal silicon technology suffered from

periodic raw material shortages and price spikes, high capital cost/capacity ratios, and module efficiencies that did not in general justify the relatively high processing costs. Polycrystalline silicon technology suffered from very low efficiencies and an immature industrial base with respect to ingot casting equipment. Thin film technologies were in a very preliminary laboratory phase.

Thirdly, and perhaps most importantly, the utility industry was firmly rooted in a conventional business concept based entirely on large central generating facilities, and ascribed little or no incremental value above base load energy costs to relatively small, distributed "peak shaving" PV systems.

The present PV market view differs significantly from the historical precedent of the past decade. Traditional industrial applications now comprise a relatively small portion of the total market for PV systems. Remote consumer applications such as lighting, water pumping, and refrigeration constitute the largest and fastest growing market segment. A profound paradigm shift taking place in the utility industry could create a significant market opportunity for PV systems. Rather than replacing central fossil fueled or nuclear generation facilities, small PV systems deployed at the outer extremities of the grid are being designed to manage demand profiles, defer transmission hardware upgrades, and support the electrical service quality (voltage, power factor, etc.) during periods of peak demand.

D. CONCLUSION

In contrast to the situation at the beginning of the last decade, the photovoltaic industry finds itself today in a position to materially contribute to the energy needs of both the developed and developing countries.

In the developed world, the most exciting market opportunities for PV products are in the emerging utility applications. In one scenario, PV systems of between 250 and 1,000 peak kilowatts, most likely employing tracker-mounted PV panels, will be installed at the outer extremities of the existing transmission grid. In this case, module efficiency is a factor of key importance, bearing on up to 80% of complete installed system costs. Siemens Solar Industries' single crystal silicon Czochralski (Cz) technology provides the highest efficiency of any commercially available PV module, and is thus a leading technology for this application.

One of the possible technology evolution paths relevant to the emerging utility market leads toward concentrating photovoltaic modules. This path is consistent with the use of tracking collectors, the probable range of geographic deployment, and the primacy of module efficiency in system economics. The flat plate Cz technology base that is the subject of this report is also appropriate to low concentration systems.

Thus, an existing large Cz flat plate capacity could be significantly leveraged by application to concentrator systems as technology and market development warrant (e.g. a 10 MW/year flat plate Cz factory becomes a 150 MW/year $15\times$ concentrator cell factory).

In the developing world, photovoltaic systems will allow a broad spectrum of off-grid rural consumers to increase their standard of living. The sale, distribution, and technical support systems required to service this diffuse customer base have been established and trained. Appropriate balance of system hardware has been identified, qualified, and sourced, in many cases by local systems integrators. The key driver to expand this market is therefore the development and high-volume manufacture of low cost (per watt), moderate efficiency flat plate PV modules. Siemens Solar Industries' CuInSe_2 (CIS) technology is a leading candidate to fulfill these product requirements.

Within the context of the PVMaT program sponsored by the U.S. Department of Energy, this report details a number of approaches to accelerate the cost effective implementation of significant advancements in both single crystal Cz silicon and thin film CuInSe_2 technologies.

III. CRYSTALLINE SILICON MANUFACTURING TECHNOLOGY

A. OVERVIEW

Single crystal silicon technology is the backbone of the current photovoltaics manufacturing operations at Siemens Solar Industries (SSI). In the past 24 months, SSI has upgraded its crystalline silicon manufacturing capacity by approximately 75%, reflecting our confidence in the long-term viability of this technology.

Many segments of the multifaceted photovoltaics market evaluate products by a simple cost per watt figure. As with any photovoltaic technology, SSI's high-volume crystalline silicon module manufacturing processes embody a balance between the desire to maximize module efficiency (watts per area) and the need to minimize cost (cost per area). Factors that tend to support the former objective include the high minority-carrier-lifetime wafers, sophisticated junction formation, advanced antireflection coatings, and low-coverage contacting techniques. Factors supporting the latter goal include higher throughputs, higher yields, higher materials use efficiency, and lower cost of materials and supplies.

This balance of efficiency and cost is dynamic. The balance changes in response to new suppliers bringing on alternate sources of raw material, production equipment suppliers constructing new generations of equipment, process engineers developing improved processes, and production operations personnel increasing yields and decreasing costs. Many such improvements have been made in the decade since the core of SSI's crystalline silicon manufacturing facility was constructed. Therefore, substantial improvements both in terms of higher efficiency, higher production volume, and lower cost can be made to the present process.

First of all, higher Czochralski (Cz) crystal pulling speed, alternate strategies for packing the initial silicon "charge", and recharge of the silicon melt can significantly increase the throughput of existing crystal growers. Development and implementation of magnetic melt stabilization techniques, improvement of the "hot zone", and use of alternate crucible materials can result in Cz wafers having markedly higher minority carrier lifetimes, which in turn result in higher cell efficiencies.

Secondly, the substitution of wire saws for conventional internal diameter saws can allow many more wafers to be cut from a given amount of ingot, thereby substantially increasing throughput and decreasing wafer cost. Development of equipment specially designed to handle the thinner wafers in high volume downstream processes can ameliorate the mechanical yield loss that might normally accompany a move to thinner wafers.

Third, advanced cell processing techniques that capitalize on the higher wafer quality can result in substantial cell efficiency improvements. Several significant innovations in this area over the past five years have served to recalibrate upwards previous expectations as to cost-effective, mass-production efficiencies achievable.

Fourth, lower cost, higher throughput automated assembly approaches to cell stringing and encapsulation, as well as module electrical termination and mounting, can appreciably reduce the cost of PV modules.

B. PRESENT MANUFACTURING CAPABILITIES AND PROCESS SEQUENCE

The basic manufacturing process consists of growing monocrystalline silicon ingots by the Czochralski method, cutting wafers from these ingots, and forming *p-n* junctions to make photovoltaic cells. The cells are then metallized, soldered into circuits, and laminated and framed into a module. A majority of the processes are performed manually in the present process fabrication sequence (Fig. 3-1). The equipment used for cell production is for the most part off-the-shelf technology common in the semiconductor industry. Conventional crystal growers, wafer saws, diffusion furnaces, and screen printers are used. A variety of specialized custom-designed equipment is used in the circuit soldering and the module assembly and packaging steps.

The basic geometry and materials of construction of present-day Cz modules are substantially the same as when Cz modules began production in 1977 (Fig 3-2). Over the past decade, this module design has become the de facto industry standard. The current-voltage curve for a standard model M55 module is shown in Fig. 3-3. The active area efficiency is approximately 14%, and the total area efficiency is approximately 12.4%, the highest module power density presently commercially available in significant quantities.

Crystalline silicon module production capacity at Siemens Solar Industries is at present approximately 10 megawatts per year. Production costs for this module are shown in Fig. 3-4. Significant cost reductions are possible through the implementation of improvements described in this report.

C. SILICON CRYSTAL GROWTH TECHNOLOGY

1. Current Technology

At present single crystal silicon ingots are grown by the Czochralski method. The silicon source material is a combination of high-purity "virgin" material purchased directly from silicon refiners and lower purity "remelt" chunks reclaimed from the

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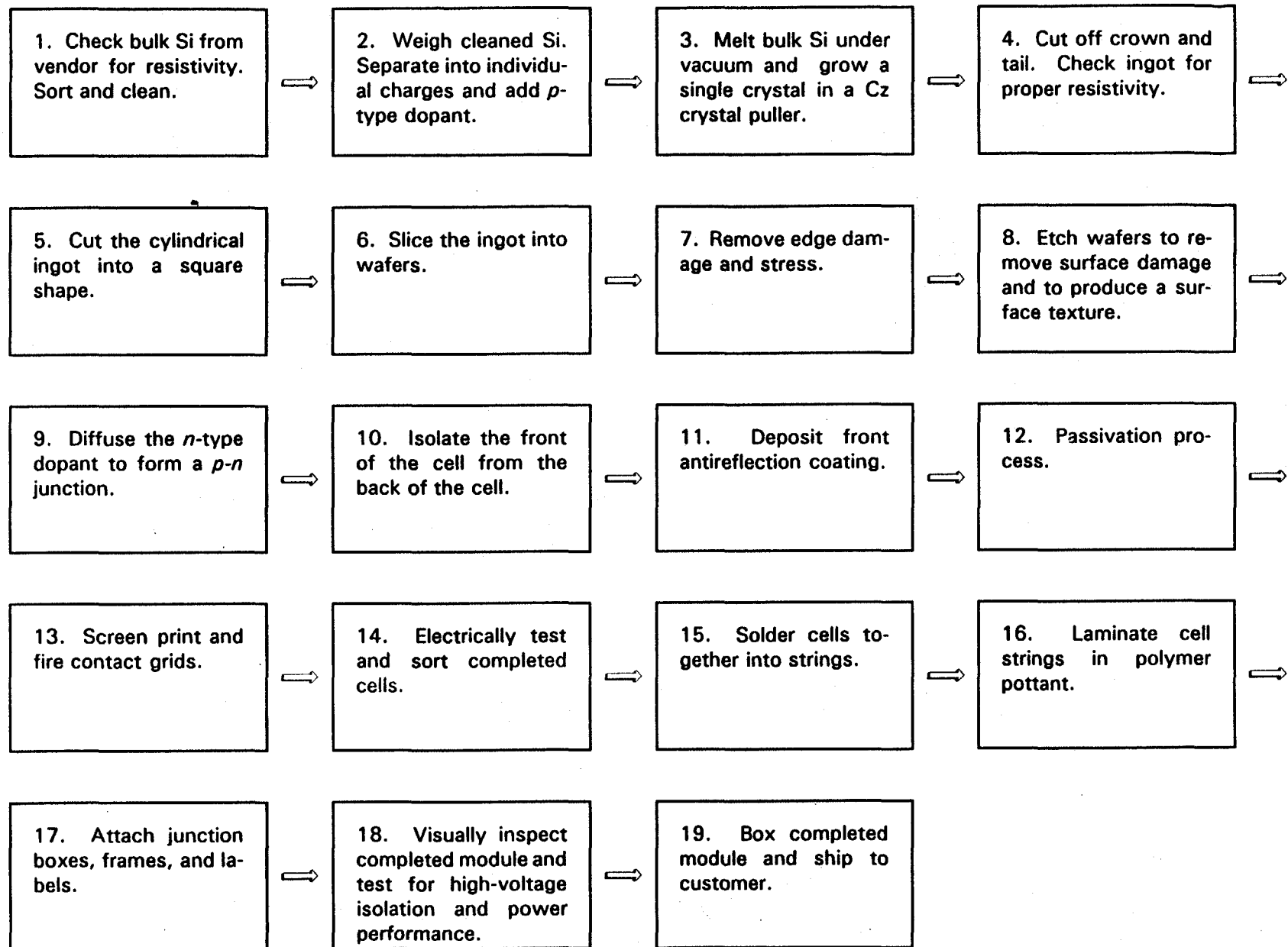


Fig. 3-1. Siemens Solar Industries' present crystalline silicon module production sequence.

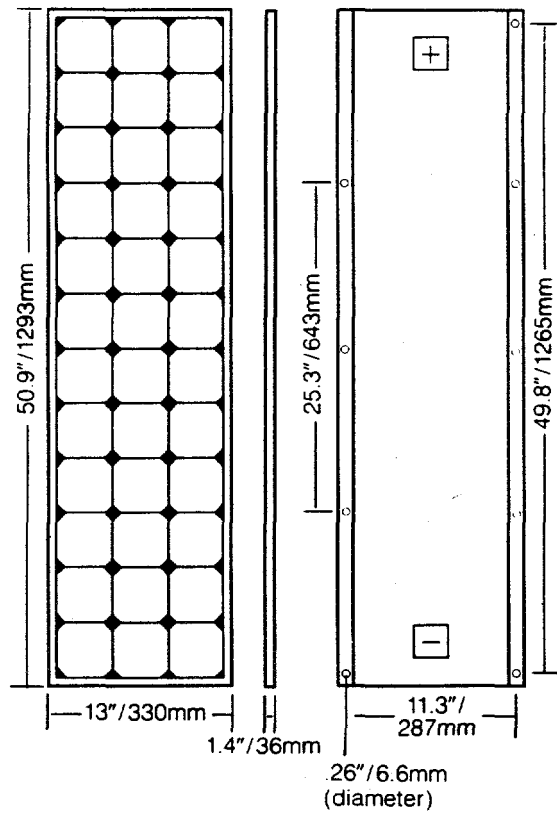


Fig. 3-2. Geometry and materials of construction for the M55 module.

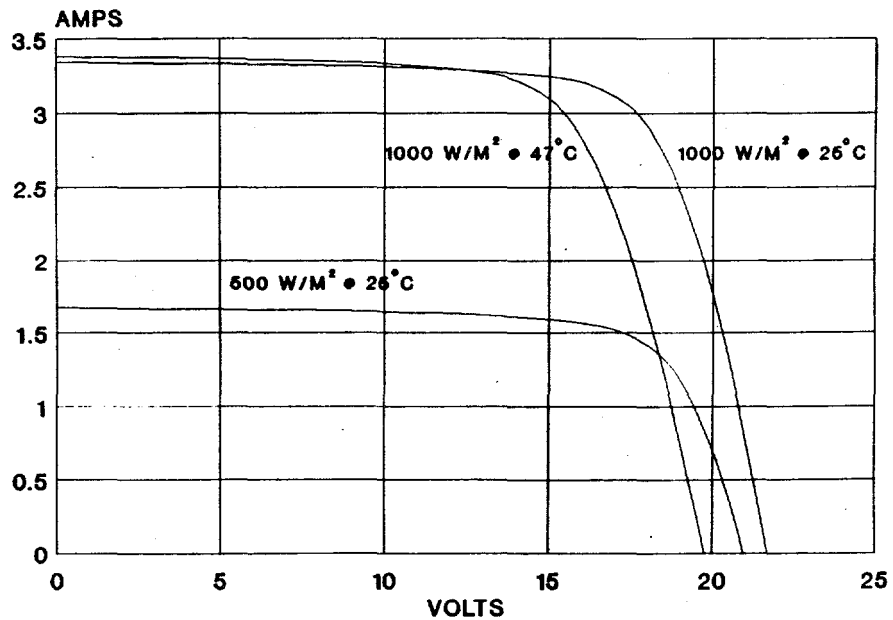


Fig. 3-3. I-V curve for a standard model M55 module.

integrated circuit industry.

The polycrystalline silicon chunks are cleaned, sorted, and packed into quartz crucibles. The packed crucibles are loaded into commercial Cz growers, and an ingot approximately 5 1/2 inches in diameter is "pulled" at a linear pulling speed of about 1 mm per minute. The complete load-to-load crystal growth cycle requires about a day. Approximately three-quarters of the polycrystalline source material is contained in the usable portion of the single-crystal ingot, and most of the balance is recycled.

Normal Cz growth conditions result in growth of "full term" ingots, which at the end of growth are properly tapered as they are removed from the Si melt. A plot of cell short circuit photocurrent I_{sc} as a function of wafer location in the ingot shows uniform performance throughout a full term ingot (Fig. 3-5). The left to right direction on the figure represents moving from the bottom towards the top of the ingot. The other cell parameters, V_{oc} and fill factor, show identical trends.

A "lost structure" ingot can result when the growing ingot loses crystal structure due to a perturbation during growth such as an oxide flake in the melt colliding with the growing ingot or an interruption of furnace power. In a lost structure ingot, I_{sc} decreases in the bottom portion of the ingot (Fig. 3-6). Similar losses occur in V_{oc} and fill factor. The primary cause of this performance decrease is the presence of slip dislocations. In Fig. 3-6, zero is the point of initial occurrence of lost structure in the ingot. The data thus indicate that the slip dislocations propagate back into the grown ingot. Optical beam induced current (OBIC) images of cell areas with slip dislocations show dark cross-hatched lines that are areas of reduced photoresponse associated with the slip dislocations (Fig. 3-7).

In the absence of slip dislocations, the minority carrier lifetime of the Cz wafers depends on the nature of the electronic defects. Through a collaborative research program established in July 1989 with the Sandia Photovoltaic Device Fabrication Laboratory, photoconductance decay lifetime measurements and calculations based on the diode reverse saturation current J_0 ¹ of our 1 ohm-cm, *p*-type Cz wafers

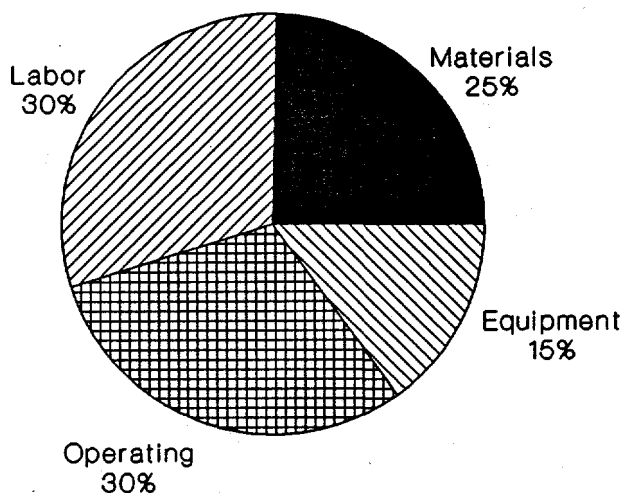


Fig. 3-4. Module manufacturing costs by expense category.

¹P.A. Basore and B.R. Hansen. *Proceedings 21st IEEE Photovoltaic Specialists Conf.*, pp. 374-379, May 21-25, 1990.

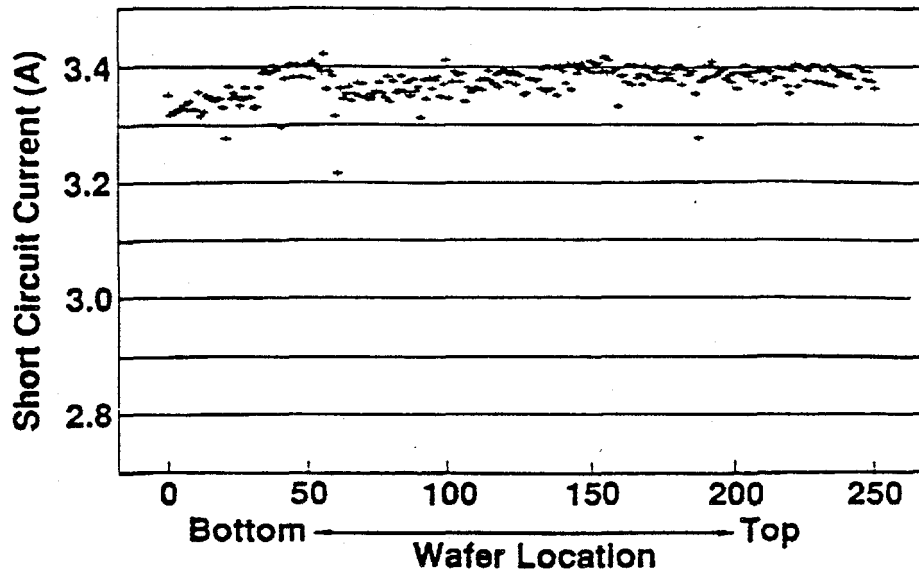


Fig. 3-5. I_{sc} versus wafer position for a "full term" Cz ingot.

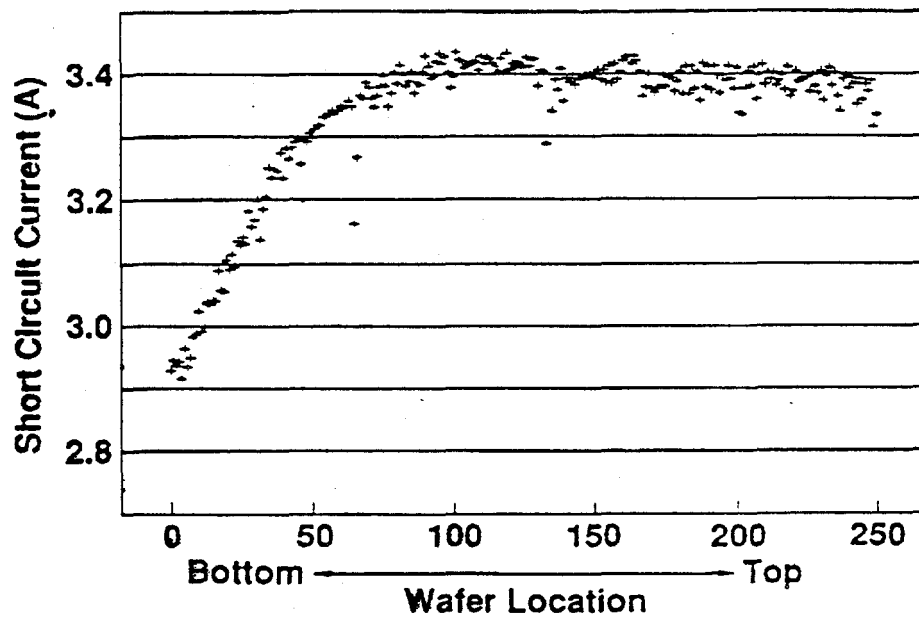


Fig. 3-6. I_{sc} versus wafer position for a "lost structure" Cz ingot.

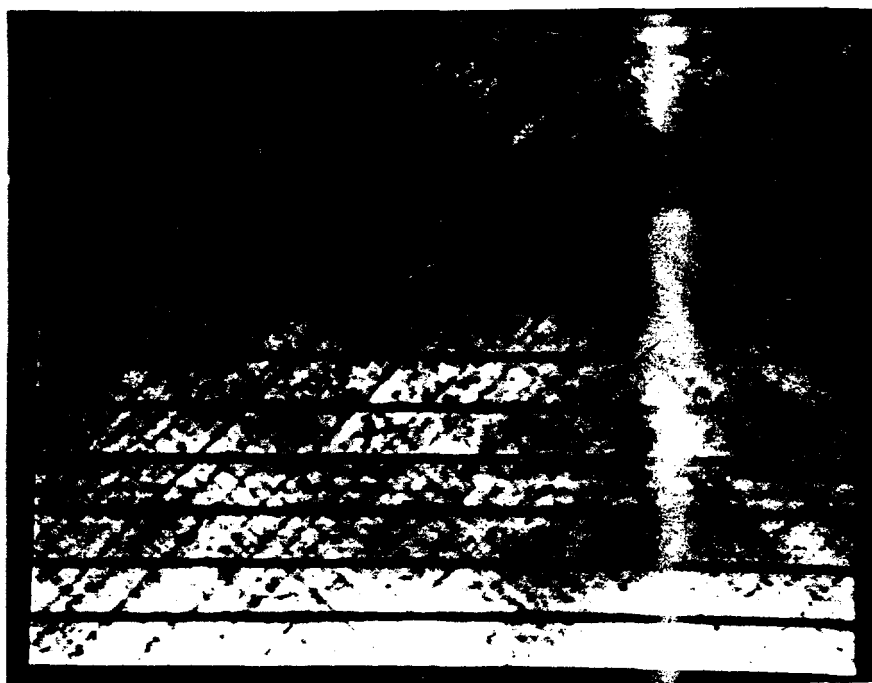


Fig. 3-7. OBIC images of cell areas showing slip dislocations.

indicate as-grown Si ingot material has a minority carrier lifetime of about 4 microseconds. High oxygen concentration and possible impurities from the polysilicon source material and grower contamination contribute to these low lifetimes. In-house Fourier transform infrared absorption analysis indicates high oxygen concentrations of 30 ppm or $1.5 \times 10^{18} \text{ cm}^{-3}$ in our Si ingots. These high oxygen contents correlate with reduced minority carrier lifetimes as noted by B.L. Sopori[†].

2. Improvements, Benefits and Challenges

Significant process and equipment improvements in Cz crystal production are possible. These improvements will increase throughput, lower costs and improve quality. Improvements can be broadly categorized as Process Development and Equipment Development.

a. Crystal Growth Process Development

Crystal growing throughput can be increased by eliminating ingot "sections", by increasing the linear crystal pulling speed, and by increasing the amount of silicon in a crucible charge.

Growth of a single "full term" ingot from a melt is the most efficient utilization of time and materials. Less than full term ingot sections can occur when disruptions such as melt inclusions or temperature fluctuations cause the growing ingot to lose crystallographic structure. If ingot growth is aborted due to loss of crystal structure, growth of a second ingot section from a given melt is attempted. In some cases, problems with the second ingot section would result in an attempt to grow a third ingot section. In the worse case, an entire ingot may be unusable due to formation of multiple crystals. Even for single crystal ingots as described in the previous section, lost crystal structure introduces slip dislocations that compromise the quality of wafers from the lower section of the ingot.

One way to decrease the frequency of ingot sections is to minimize the incorporation of oxides and other impurities into the melt. Alternative source materials and preparation techniques will be evaluated to eliminate ingot sections. A 15-20% increase in effective ingot production rate could result from the elimination of sections and reduction of heat/cooling and "seeding" cycle time. This is highly leveraging in the impact on production cost because of the high value content of crystal growing.

Initial results on higher ingot pull speeds and increased polysilicon charge size have

[†]B.L. Sopori. *Proceedings of the 20th IEEE Photovoltaic Specialists Conf.*, pp. 591-596, Sept. 26-30, 1988.

been promising. Electro-mechanical problems with the older crystal growers in the Camarillo factory have been resolved and new growers have been installed in the Vancouver production facility to facilitate higher pulling speeds. Ciszek¹ reports that typical Cz ingot growth rates range from 1 mm/min (2.4 inches/hour) to 2 mm/min (4.7 inches/hour). Present linear pulling speeds could be increased 20-80% with no significant loss in crystal quality. Figure 3-8 shows the grower throughput in inches per hour as a function of the ingot pull rate for the cases of one full term ingot per melt and two ingot sections per melt. This higher linear pulling speed translates to a 10-30% increase in overall average ingot length production rate.

The productivity of a Cz grower can be further increased by increasing the amount of silicon in a crucible charge. Larger charge sizes will be explored using the higher packing density possible with small-diameter silicon source material purified using the fluidized-bed process. A 5-10% increase in charge size would increase the effective cycle-to-cycle ingot production rate by approximately an equal amount provided that faster linear pulling speeds offset longer set-up times. Initial trials with larger polysilicon charges using fluid bed material have been successful, but the control of oxide contamination resulting from larger surface area of fluidized bed material must be resolved.

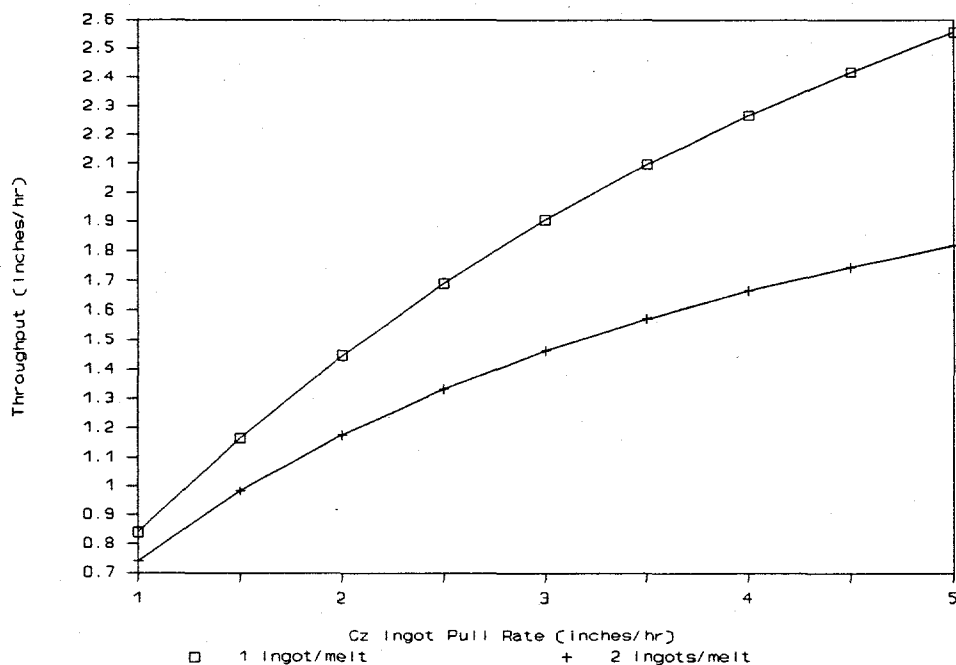


Fig. 3-8. Cz grower throughput.

¹T.F. Ciszek. *Proceedings of the 20th IEEE Photovoltaic Specialists Conf.*, pp. 31-38, Sept. 26-30, 1988.

b. Crystal Growth Equipment Development

Crystal growing throughput and ingot quality can be increased by alternative crucible materials, grower "hot zone" improvements, melt recharge, and magnetic Cz techniques.

Alternative crucible materials and quartz crucible coatings are increasingly common in Cz crystal production. The potential advantages of alternative crucibles and coatings include the reduction of disruption of the silicon melt by quartz particles; such disruptions cause approximately half of the lost structure ingot sections produced at present. Alternative crucible materials and crucible coatings are expected to decrease by 25% the amount of ingot lost to silicon melt contamination by the crucible. The direct material costs of these alternatives will be evaluated in comparison with the improvements in ingot yield and effective growth rate.

Development of an improved hot zone in the Cz growers will improve the uniformity and stability of the temperatures of the melt and ingot and will enlarge the window of acceptable parameters for single-crystal growth. This will increase production yields of full term ingots and increase effective growth rate.

A significant fraction of the crystal growing cycle is consumed by grower set-up steps. By recharging the silicon melt in the crucible without re-initiating the entire growing sequence, it is possible to save considerable set-up time and to reduce the indirect materials cost of replacing the crucible, which comprises a large portion of the operating expense in this step.

Siemens Solar Industries has substantial previous experience with silicon recharge equipment and processing using single hoppers of solid silicon feeding each grower. Past efforts (1984-85) were limited by excessive oxide contamination of the melt by the polysilicon silicon material used in the recharge process. The present effort is directed toward using solid silicon source material with less surface oxide.

An alternative method of melt recharge is to melt silicon in a vessel separate from the grower and to flow molten material into each grower. One advantage of this method is the "skimming" effect of the impurities floating on the top of a central molten bath, while the molten silicon extraction takes place from the bottom of such a vessel. Molten recharge could significantly reduce the oxides and contamination introduced during the recharge operation, and would permit recycling of raw silicon "pot scrap" now discarded.

The net impact of melt recharge could be a 5-10% increase in ingot production rate and about a 5% decrease in ingot cost.

Magnetic Cz crystal growth is increasingly being used in the semiconductor industry to control oxygen and other impurities through the ingot. Lower oxygen content in solar grade wafers will increase minority carrier lifetime and ultimately the efficiency of the solar cells produced. An added benefit of the magnetic Cz equipment is reduced turbulence of the melt, which improves yields of full-term, dislocation-free ingots. Initial inquiries to equipment manufacturers confirm that an existing Cz grower can be retrofitted with magnetic Cz capability. The capital investment will be evaluated in comparison with cell/module efficiency and ingot production rate.

The impacts of magnetic Cz crystal growth could be an order of magnitude increase in minority carrier lifetime, a relative increase of 20-30% in cell efficiency when combined with the improvements in cell processing described below, and a 5% increase in ingot production rate.

3. Resources Required to Develop Improvements and Realize Benefits

The overall improvement in crystal growth could be up to a 75% increase in grower productivity and up to a 30% decrease in ingot cost.

We propose to devote one experienced Cz equipment design engineer and one Cz process engineer to these development tasks. In addition, one existing crystal puller will be required for the development work along with an operator. Expenses for prototype equipment will be required.

This work will require about 18 months at a cost of approximately \$1 million. These costs include \$200,000 in labor, \$300,000 in materials, and \$500,000 in experimental equipment modifications.

D. THIN WAFER TECHNOLOGY

1. Current Technology

At present, single crystal silicon ingots are cut into square wafers in a three-step process. The first step is to slab the cylindrical ingot into a block with a nearly square cross section. The second step is to saw the block into individual wafers. This sawing process is at present done with standard internal diameter (ID) saws using diamond-imbedded blades. The third step is to grind the edges of the wafers to remove minor edge damage and to relieve mechanical stress.

This current wafering technology converts approximately half of the cylindrical ingot into square wafers. The balance is lost as sawing kerf or reclaimed as ingot slabs that are remelted in subsequent crystal growth runs.

2. Improvements, Benefits and Challenges

Thin wafer technology has the potential for dramatically increasing the PV cell/module manufacturing capacity possible from a fixed quantity of silicon source material and a fixed quantity of crystal growing capacity. Two general options for thin wafer technology are possible. First, it is possible to use the existing ID saws to cut thinner wafers, but the mechanical yield would decrease sharply if wafer thicknesses were reduced much below about 0.020 inch. Since a typical ID saw consumes about 40% of the slabbed ingot as kerf loss, a 10-20% reduction in wafer thickness would yield only a 6-12% increase in wafers per unit length of ingot. Also, 10-20% of the as-sawn thickness is generally etched off in order to remove mechanical damage. When the kerf and damage removal losses are combined, the capacity increase possible from thinner wafers cut using ID saws is perhaps 5-10%.

A second option for thin wafer technology is wire saw equipment where the ingot is sliced using a high-tension wire that pulls an abrasive slurry across the silicon crystal. Wire saws generally employ multiple wire paths to simultaneously cut many wafers from a single ingot.

The kerf loss of wire saw technology is typically about half that of ID saw technology, and it is possible with the wire sawing technique to significantly reduce the amount of residual mechanical damage and hence the damage removal losses. A comparison of the wafer yield per inch for ID and wire saws is presented in Fig. 3-9 for different cell thicknesses. For the present cell thickness, wire saws would increase the number of wafers cut per unit length of ingot by about 35%. By reducing wafer thickness, wire saws could increase wafer output per ingot by upwards of 150% without unreasonable demands on wafer strength using existing techniques. On the whole, wire saw technology could increase cell/module manufacturing capacity by 25-125%.

Overall, wafer output per ingot and hence module production volume could more than double as a result of wire saw technology.

Wire saw technology has advanced dramatically during the past ten years. The equipment currently commercially available appears capable of large scale thin wafer production. Though the mechanical fragility of thin wafers will likely require improvements in wafer handling and adjustments to the cell processing procedures, the wire sawing process itself is the primary challenge.

Exploration and implementation of wire saw technology will involve three phases over two years: the evaluation of a prototype wire saw, the identification of the optimum balance of wafer thickness and process yield, and the transition to thin wafer technology in high-volume production.

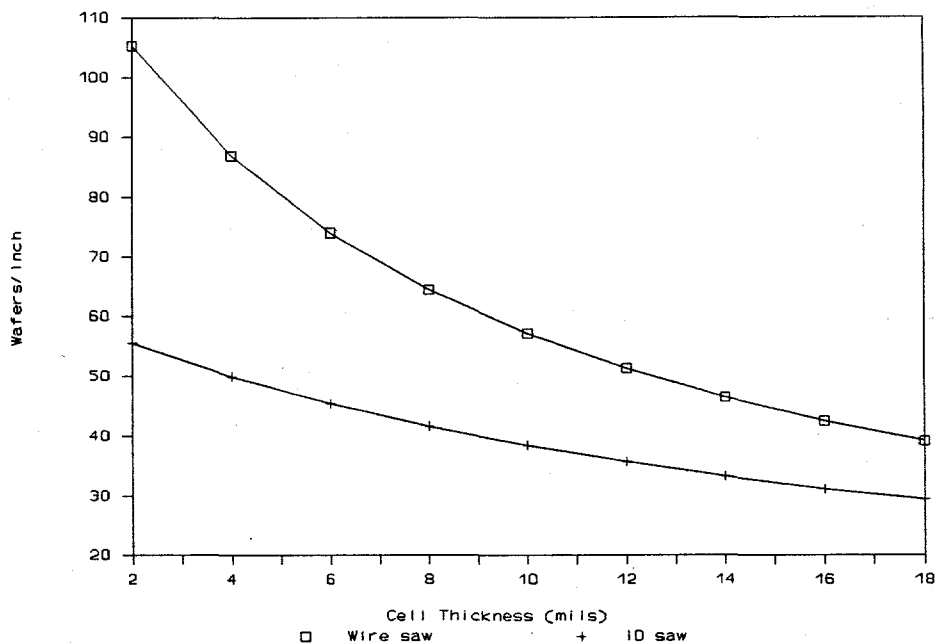


Fig. 3-9. Wafer yield for wire saw and ID saw.

The first phase involves a practical evaluation of a prototype, commercially available wire saw. The equipment performance will be verified, and the wafer quality will be evaluated. Direct material consumption and costs will be quantified.

The second phase involves the evaluation of thin cell fabrication using current cell processes and production equipment. A matrix of thin wafers will be processed to identify the optimum thickness of as-cut wafers. The mechanical strength and device performance will be evaluated as a function of thickness. Problems due to processing, equipment or handling will be explored. Wafer cleaning, wafer texturing, junction formation, contact application, cell interconnect, and packaging/module fabrication complications will be addressed. Alternative process and equipment designs will be considered.

The third phase will implement the transition to high-volume thin wafer production.

3. Resources Required to Develop and Realize Benefits

Thin wafer technology has the potential for reducing the manufactured cost of solar cells by up to 30% in three years. Approximately \$400,000 over 24 months will be required to complete this task. Two full-time engineers and one full-time technician will be required to evaluate the wire saw machinery and to coordinate the cell processing evaluation.

E. CELL PROCESSING TECHNOLOGY

1. Current Technology

Cell processing is the sequence of tasks necessary to convert a bare silicon wafer into a complete solar cell. The present cell processing sequence begins with a thorough cleaning to remove all residual chemical and particulate contamination from the wafer sawing process. Next, the wafers are isotropically etched to remove the mechanical damage due to sawing and are anisotropically etched to form a surface texture of microscopic pyramids to maximize light-trapping in the complete cell. Metallic impurities are gettered and the *p-n* junction is formed in standard atmospheric-pressure tube furnaces. An antireflection coating is applied and the cell is treated to passivate the electrically active surfaces. Electrical contact grids are applied using screen-printed metallic glass pastes.

At present cell processing is semiautomated. Wafers/cells are automatically loaded, processed, and unloaded from processing equipment, but wafer/cell transfer between machines is done manually.

This basic cell processing sequence produces 14-16% total area efficiency cells as measured at 1 sun illumination. Approximately 6 million 4-inch-square cells are processed each year. One cause of reduced cell efficiency is the presence of slip dislocations as described in the above section on silicon crystal growth technology. The light current-voltage (I-V) curves (under 100 mW/cm² ASTM 1.5 global spectrum) for Type A (no slip dislocations) and Type B (slip dislocations present) are compared in Fig. 3-10. The Type A cell is 15.6% efficient with a 32.9 mA/cm² J_{sc} , 621 mV V_{oc} , and 0.763 fill factor based on a 103.5 cm² total area. In contrast, the Type B cell is 14.0% efficient with a 30.6 mA/cm² J_{sc} , 607 mV V_{oc} , and 0.754 fill factor. The lower J_{sc} for the Type B cells results from loss of long wavelength response due to a reduced effective minority carrier diffusion length caused by the slip dislocations (Fig. 3-11).

2. Improvements, Benefits and Challenges

Substantial opportunities exist to reduce costs by improving cell processing equipment and by developing new or improved processing methods. We propose a two-part development program consisting of near-term improvement of the present manufacturing techniques and the parallel initiation of a longer term "quantum leap forward" program to develop high efficiency cell processes in manufacturing.

Near-term improvements of present manufacturing processes will focus on the significant and varied opportunities for efficiency enhancements, cost reductions, and

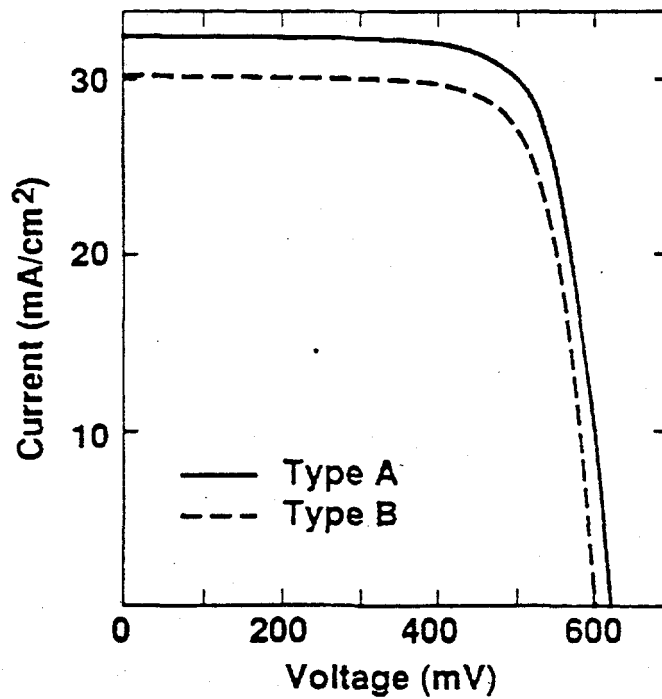


Fig. 3-10. Light I-V curves for Type A and Type B Si cells.

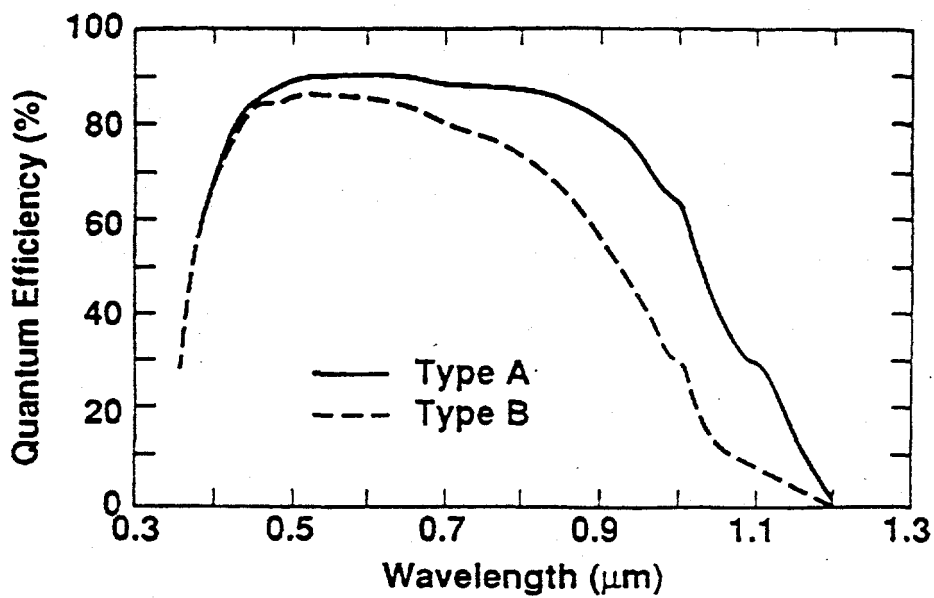


Fig. 3-11. Spectral response for Type A and Type B Si cells.

volume increases that have been identified as possible using the existing factory equipment and work force. The longer term development program aimed toward implementing a quantum leap forward improvement in cell efficiency in high-volume production will focus on new techniques for junction formation and electrical contact formation.

To fully capitalize on this opportunity, we plan to enlist the participation of non-PV industrial partners and the academic community.

Cell efficiency strongly leverages the cost per watt of the completed module. The cell processing improvements envisioned here are capable of increasing the efficiency of cells by 20-30% and reducing module cost per watt by a comparable amount if cell processing costs are not substantially higher.

The specific improvements and methodology for development are described below.

a. Near-Term Improvement of Present Manufacturing Processes

i. Etching

The wafer-to-cell process begins with a series of etching processes aimed at cleaning and texturizing in preparation for the subsequent junction diffusion step. A series of etches are employed to pre-clean the wafers, to remove the saw damage, to texture to create a microscopically pyramidal surface structure to minimize reflective losses, and to clean the surface of contaminants in preparation for junction diffusion.

The etching processes are extremely important in determining cell efficiency. For example, a bare silicon wafer in air reflects about a third of the incident sunlight, but with proper texturizing this can be reduced by a factor of three. Inadequate cleaning prior to diffusion can leave impurities that cause high trap state densities and high recombination losses with a resultant loss of cell efficiency.

Automated handling will be implemented to better control the process of the wafers through the etching sequence. Etching effectiveness will be evaluated by microscopic examination, by reflectivity measurements, and by comparison of the final cell electrical performance relative to a control group of cells processed by baseline methods. These experiments will guide the design of automated etching equipment. Automated equipment will reduce the direct labor cost by 50% and improve safety since the direct handling of wafers will be eliminated. Materials consumption will be reduced by the additional precision and reproducibility possible with automated equipment.

Improved fixturing and etchant mixing will be implemented to improve the uniformity

of the etching process. At present local variations in etching rate results in up to a 5% loss in cell power and requires that the etching process be prolonged to assure minimum etching on all areas of the wafer. Improved uniformity will increase average cell efficiency and may decrease etchant consumption.

ii. Diffusion Process

The present diffusion process is a batch process in which wafers are loaded into quartz boats, inserted into a large diameter quartz tube furnace, heated to between 800-1000°C, and exposed to gases and vapors containing oxygen and chlorine to getter out metallic impurities and containing phosphorous to create a $p-n$ junction via thermal diffusion of phosphorous into the silicon.

This batch diffusion method is reliable, but it requires significant labor for parts handling and furnace loading and unloading. Preliminary studies in collaboration with Sandia National Laboratories indicate that the present diffusion process is not yet optimized. A substantial amount of electrically inactive phosphorus is present in the emitter layer, reducing the minority carrier lifetime and as a consequence lowering both the spectral response at shorter wavelengths and the cell V_{oc} due to increased carrier recombination. Studies will be carried out to optimize the present diffusion process, evaluating dopant and carrier gas flow rates, diffusion times and temperatures, and heating and cooling rates.

In addition, we propose to evaluate in-line, continuous-transit diffusion equipment in which each wafer passes through discrete zones for heat-up, temperature stabilization, dopant deposition, dopant drive-in, and cool-down. The gas flow characteristics will be configured to uniformly flow across each wafer surface, rather than in the complex, highly non-uniform patterns inherent to a confined, short tube furnace heavily loaded with many wafers. In this manner, each wafer will experience the same thermal and gas kinetic conditions.

One approach to continuous-transit diffusion that will be examined is a flow-through diffusion tube. The performance of such a continuous-transit process will be evaluated by a series of experiments in a standard diffusion tube furnace. By carefully cleaning all of the furnace fixturing, and extensively purging with inert gas before wafer entry, the pre-diffusion exposure to oxygen and phosphorous can be minimized. By selecting matched wafers, the first-in/last-out versus last-in/first-out wafer differences can be measured. The effect of flow uniformity can be estimated by greatly decreasing the number of wafers in a given batch (i.e., by greatly increasing the wafer spacing). The wafers can be oriented either parallel or perpendicular to the tube axis and gas flow pattern. The benefits of a theoretically continuous-transit diffusion tube will be deduced by determining the best performance obtainable from

idealized, localized sampling experiments in a fixed-position batch tube.

A second approach to continuous-transit diffusion that will also be examined involves heating in a high-temperature, atmospheric-pressure belt furnace. Such a process offers the advantages of being a continuous process and one-sided. Another potential benefit is that the diffusion can be controlled in specific zones. We have negotiated to perform these in-line diffusion experiments in collaboration with a major furnace vendor.

iii. Cell Antireflective Coatings

It is well known that cell photocurrent can be increased by antireflection (AR) coatings, by surface passivation, or by a combination of an AR coating and passivation. In the present production process, an AR coating of TiO_2 is applied to each wafer. Following this process, the wafers are further treated to passivate potential recombination sites and to enhance the optical properties of the AR coating. We have arranged to experimentally evaluate AR/passivation combinations in collaboration with university researchers. Polished and textured wafer samples for each process step and for incremental process sequences will enable measurements of refractive indices, coating thicknesses and reflectance as a function of wavelength. Carrier concentration versus depth measurements, and SIMS and Auger composition analysis of the antireflective coating, the dopant diffusion gradient, and the passivation layer will be done.

We further propose to explore multilayer AR coatings that would minimize reflective losses over a wider wavelength spectrum. We have arranged to collaborate with a manufacturer of printable AR pastes, diffusion pastes and fritted silver pastes on this exploration. One particularly attractive concept would employ a doped AR paste which would offer better electric conductivity than the existing antireflective film.

The study of multilayer antireflective films is very specialized and complex. We have arranged to collaborate with a university on this study. The effort will involve liquid spin-on, printed paste, CVD, and the vacuum deposition of various films on polished silicon wafers and on active, textured and diffused wafers and cell. In addition, we plan to have the university examine the increase in photocurrent observed when a cell is laminated even though the glass surface reflection and transmission loss would suggest a photocurrent reduction.

iv. Cell Metallization Process

The present production process for metallizing cells is based on the use of fritted silver pastes applied by screen printing and sintered using a high-temperature, atmospheric-

pressure belt furnace. This same general process is in use by many PV manufacturers both here in the U.S. and abroad. Although a multitude of paste formulations are commercially available, the subtleties of the firing process, of cell surfaces, and of post-firing treatments severely complicate the evaluation of alternative formulations.

We propose to conduct a paste development program centered around a single, commonly used fritted silver paste. We propose to systematically vary the paste formulation. The variables to be addressed include the glass content, the glass chemistry, the dopant concentration, and the paste rheology. We have arranged to collaborate with a major paste vendor on these experiments.

v. Cell Firing Optimization

With fritted silver pastes, high temperature firing is required to bond the silver particles both to each other and to the wafer surface via melting of the glass frit. It is believed that opportunities exist for significant improvement, particularly if this effort is coupled with a paste development program.

Some of the firing experiments will be performed on our production furnace, but we have arranged for the bulk of the experiments to be performed in collaboration with two furnace manufacturers well known to the PV industry. Each of these major manufacturers has research lab furnaces capable of encompassing the complete range of firing methods and conditions.

b. Longer-Term Development of High-Efficiency Manufacturing Processes

A longer-term development effort aimed at implementing high-cell-efficiency processes in high-volume production will be explored in parallel with near-term improvements to the existing cell processes. The goal is to increase the average production cell efficiency from 14-16% to around 20%.

We propose to investigate vacuum deposited metallization methods, metal oxide coatings, and plated contacts. These alternative electrical contact fabrication processes offer the possibility of higher photocurrents due to lower reflection losses and grid coverage, of higher fill factors due to lower resistive losses, and of minimization of the high-temperature firing of glass frit contact pastes. The high temperature contact firing of crystalline silicon wafers is a potential source of junction shunting and minority carrier lifetime losses. Glass frit pastes may also create excessive stresses on thin wafers and may result in lower mechanical yields. An advanced study of contacting methodologies will be performed with the primary goal of efficiency improvement and with the secondary goal of mechanical yield increases.

We also propose to explore advanced dopant diffusion techniques. A short, high temperature dopant deposition is envisioned with a very rapid drive-in time. The junction formation needs to be quickly formed in a very pure process environment, then the cell cooled to allow no contamination to be incorporated in the electronic device. This requires a fundamental change in the present diffusion process to an in-line, rapid thermal processing (RTP) technique. Existing RTP equipment will be used to validate the concepts, and prototype production equipment will be explored.

A third technology issue to be addressed in this effort will be the surface passivation techniques required to realize high cell efficiencies on thin wafers. Hydrogenation and other passivation processes will be explored to reduce surface recombination rates.

3. Resources Required to Develop Improvements and Realize Benefits

The near-term improvements in cell processing technology will require the equivalent of one full-time and one half-time manufacturing engineers, one full-time research scientist, and two full-time production technicians at a total cost of about \$500,000 for labor, materials, services over 24 months. The longer term development of high-efficiency manufacturing processes will require one full-time process engineer, one full-time research scientist, and one research technician at a total cost of about \$300,000 for labor, materials, and services over 18 months.

F. MODULE FABRICATION TECHNOLOGY

1. Current Technology

Module fabrication is a sequence of assembly and finishing steps by which individual cells are transformed into integrated, packaged modules. The present module fabrication process consists of soldering cells together into cell strings, soldering strings together into circuits, lamination of the circuits to a protective cover, attachment of a mounting frame and electrical connection hardware, and final testing and inspection.

The present module fabrication process is very materials and labor intensive.

2. Improvements, Benefits and Challenges

Substantial opportunities exist to reduce costs and increase volumes of manufactured PV modules by taking a new look at how silicon cells are packaged into integrated modules.

The direct labor and materials expenses of the present module fabrication process can be significantly reduced by developing alternative low-cost materials and module

designs and by automating the assembly and finishing processes.

Alternate module materials will be explored. Options to the existing EVA pottant, multilayer back sheet, glass front cover, extruded aluminum frame, and present junction boxes will be evaluated. Cost savings of 15-55% are believed possible.

Alternate module designs will also be explored. Since much of the module fabrication cost is relatively independent of module area, the module design is driven toward larger sizes. We propose to focus our module design and module fabrication equipment efforts on modules on the order of 8 ft² in size. Alternate module designs could reduce module fabrication materials costs by 10-20%.

Module fabrication labor costs will be addressed through automating the assembly and finishing processes. The first task of the automation effort will be to conveyerize parts transport between processing machines. The second task will be to automate the soldering of cells into strings, the "lay-up" of the back sheet, string, pottant, and cover sheet, the lamination of the lay-up stack, the attachment of junction boxes, and the installation of mounting frames. The third task of the automation effort will be to automate the testing of module power and high-pot resistance. Automation of module fabrication could reduce module labor costs by 50% or more.

The design of the module, the module assembly techniques, and automated assembly equipment appropriate for low-cost manufacturing are intimately linked. The project will combine in-house engineering resources and subcontracted industrial design and engineering resources. Specific handling and machine design tasks will be designed by outside equipment vendors. Factory lay-out and material flow tasks will be done by an outside industrial engineering firm. The designs will be implemented by in-house engineers.

3. Resources Required to Develop Improvements and Realize Benefits

Improvement of the crystalline silicon module fabrication technology will be pursued in parallel with the development of thin film CuInSe₂ module fabrication technology. The combined module fabrication development project is expected to require 18 months to complete. Two full-time research engineers, one experienced packaging/testing technician, and one experienced product design engineer will be assigned to the project. The total project cost will be approximately \$500,000 split roughly between labor and expenses for materials, prototype equipment, and services.

G. ENVIRONMENTAL ISSUES

Siemens Solar Industries is strongly committed to safeguarding the environment and

to guaranteeing safety in the work place. This proposal implements this commitment to preventing future environmental problems by minimizing the use of hazardous materials and by decreasing the quantities of waste generated by PV manufacturing.

1. Current Technology

At present, the manufacturing process for crystalline silicon PV modules requires the use of caustic liquids for etching and solvents for cleaning. Caustics are purchased as high-concentration liquids. Used caustic is recycled by an outside vendor for other uses. Solvents are purchased in bulk, and generally evaporate during use, leaving no significant liquid solvent quantity for disposal.

2. Improvements, Benefits and Challenges

Caustic and solvent usage and disposal are targeted in this proposal for significant improvement. The first goal is to decrease the volume of liquid caustic waste generated by the etching processes. At present, nearly 15% of the cell processing costs are attributed to waste and disposal. Caustic waste disposal has averaged 250,000 gallons per year at a cost near \$500,000. A significant cost reduction is possible if the waste volume can be reduced. We propose to review the industry practice and the literature, and to perform experiments to decrease the volume of liquid caustic waste by 75% by de-watering the wastes and to procure equipment that will accomplish this on a manufacturing scale.

The second goal is to decrease or eliminate the use of chlorofluorocarbon (CFC) solvents now used for cleaning processes such as flux removal after cell string soldering. CFC usage over the past three years has been steady at an average of 5000 gallons/year, but CFC costs have doubled as CFC prices have risen.

We propose to evaluate for PV module manufacturing a wide range of commercially available CFC replacements such as aqueous and non-aqueous cleansers and alternate solder fluxes. We propose to test the impacts of these options to existing CFC's for as-fabricated PV cell efficiency and long-term PV module durability. We will analyze manufacturing costs and yields to quantify the impact of these environmental issues.

3. Resources Required to Develop Improvements and Realize Benefits

The investigation of opportunities to reduce caustic wastes and eliminate CFC usage in high-volume PV module manufacturing will require approximately 20 months at a cost of about \$200,000 equally split between labor and materials.

IV. THIN FILM CuInSe_2 MANUFACTURING TECHNOLOGY

A. OVERVIEW

Thin film CuInSe_2 (CIS) photovoltaic technology is the leading new contender to provide substantially lower cost flat plate PV modules appropriate to a broad range of markets. CIS thin film technology has demonstrated in principle the capability of combining the low costs per unit area inherent to monolithic, integrated thin film module manufacturing techniques with the high power densities typical of crystalline silicon modules. This combination of low cost and high efficiency has the potential for opening significant new markets to the photovoltaic industry.

SSI's CIS technology has reached a stage of development where pilot production, and ultimately full scale manufacturing, are possible. This report details the most leveraging development tasks necessary to achieve a competitive, profitable manufacturing cost base. Achievement of these cost targets will occur primarily through engineering development of existing pilot-scale processes into commercial-scale manufacturing processes.

Significant cost leverage is possible through the efficient utilization of materials. Alternate feedstock materials and materials reclaim have strong potential for reducing direct materials costs as well as waste disposal expenses. Equipment design improvements and implementation of process diagnostics and controls are proposed to improve equipment reliability, processing speed, materials utilization, module performance, and module yields. Automation of labor-intensive steps will minimize labor costs and maximize product quality. Implementation of manufacturing process/-equipment/facility integration during the early stages of manufacturing development is proposed to attain optimum plant efficiency by facilitating smooth product flow and alternative high-density parts storage and equipment interfaces.

To remain competitive, the U.S. photovoltaics industry must press forward to remain ahead of ever-stiffening safety and environmental standards and to lead the world in setting the standards for the safe and environmentally conscious operation of large-scale semiconductor manufacturing facilities. Failure to anticipate these requirements as an inherent part of the manufacturing process would result in increased costs due to expensive retrofits and add-ons. Improvements in equipment and facility design, increased materials utilization and materials reclaim, alternate feedstock materials, efficient use of utilities and water, ergonomic work station design, and waste minimization are proposed to address these manufacturing costs.

B. PRESENT MANUFACTURING CAPABILITIES AND PROCESS SEQUENCE

CIS module production is presently in a piloting phase and is not yet as well defined as the commercial production sequence of crystalline silicon manufacturing. The basic CIS module production technology consists of fabricating thin film circuits on a glass substrate in a sequence of deposition and patterning steps of a metal electrode, the CuInSe_2 absorber, and a two-layer transparent electrode. The submodule plates are packaged into modules by lamination to a tempered cover glass followed by polymer framing. All processing is presently done manually. The step-by-step CIS module fabrication sequence is presented in Fig. 4-1. Most of the existing CIS processing equipment has been custom designed and built.

The current-voltage (I-V) curve for a 0.4 m^2 CIS submodule is shown in Fig. 4-2[†]. The module aperture area is 3890 cm^2 (3610 cm^2 active area) and the output power is 40.4 watts with a 2.52 amp I_{sc} (37.0 mA/cm^2 active area J_{sc}), 24.6 volt V_{oc} (464 mV/cell), and 0.652 fill factor, resulting in a 10.4% aperture area efficiency. The module geometry is illustrated in Fig. 4-3[†]. Prototype CIS modules under test at the SERI PV Outdoor Test Site in Golden, Colorado, changed less than 6% after 18 months of continuous outdoor exposure (Fig. 4-4^{††}), demonstrating an inherent stability of the CIS submodule circuit.

I-V characteristics for a 3.5 cm^2 active area single-junction test cell are shown in Fig. 4-5^{†††}, with 41.0 mA/cm^2 J_{sc} , 508 mV V_{oc} , and 0.677 fill factor, for an active area efficiency of 14.1%. Predicted performance for cells with these characteristics manufactured uniformly in the geometry of the CIS submodule is 51.8 watts, as summarized in Table 4-1[†].

Although CIS modules are presently not in commercial production, and thus the module production costs are not available, the commercial production costs are projected to be 25-50% of the lowest achievable crystalline silicon module costs[†]. The cost of thin film CIS modules is expected to be dominated by fixed costs during early start-up pilot operations, by materials and labor expenses in pilot production, and by materials expenses in commercial production. The anticipated representative

[†]C. Eberspacher et al. "Recent Advances in Single-Junction and Tandem Thin Film Modules Based on CuInSe_2 ." *Proceedings 10th European Photovoltaic Solar Energy Conf.*, Lisbon, Portugal, April 8-12, 1991 (in press).

^{††}J. Ermer et al. "Advances in Large Area CuInSe_2 Thin Film Modules." *Proceedings 21st IEEE Photovoltaic Specialists Conf.*, pp. 595-599, May 21-25, 1990.

^{†††}K.W. Mitchell et al. " CuInSe_2 Cells and Modules." *IEEE Transactions on Electron Devices*, 37, 2, pp. 410-417, Feb. 1990.

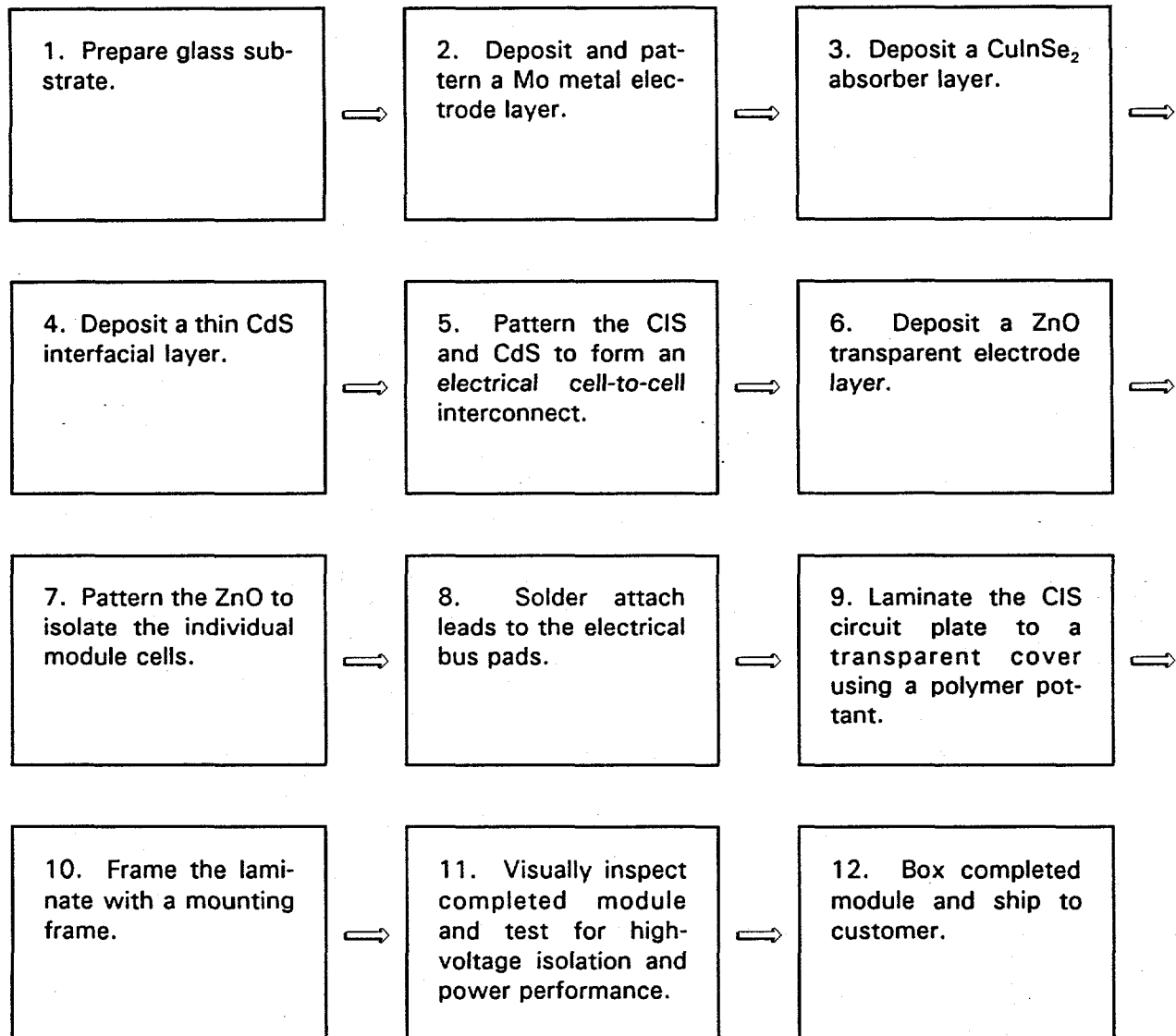


Fig. 4-1. Block diagram for CIS module production sequence.

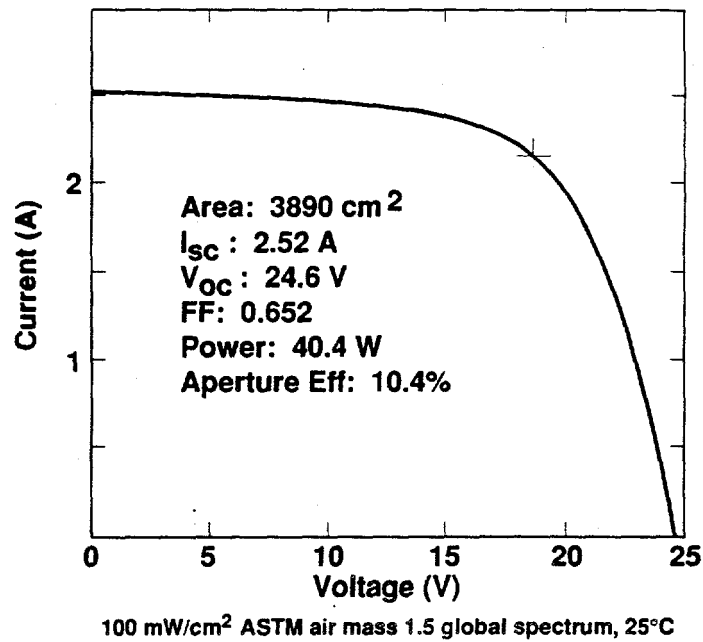


Fig. 4-2. I-V curve for unencapsulated 0.4 m² 40 watt CIS module.

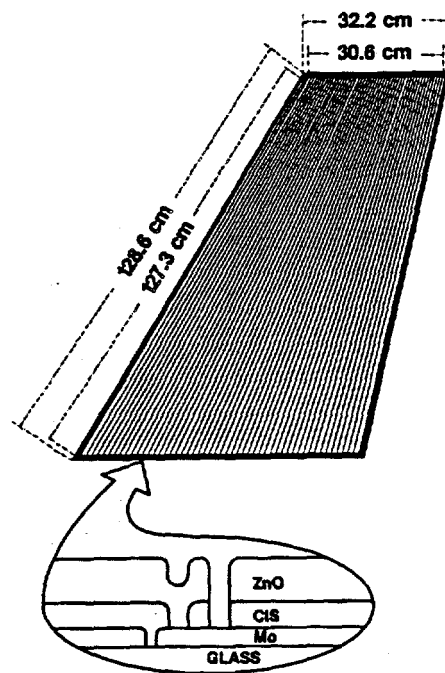


Fig. 4-3. Basic design of 0.4 m² CIS module. The details of the integrated interconnect are shown in the inset.

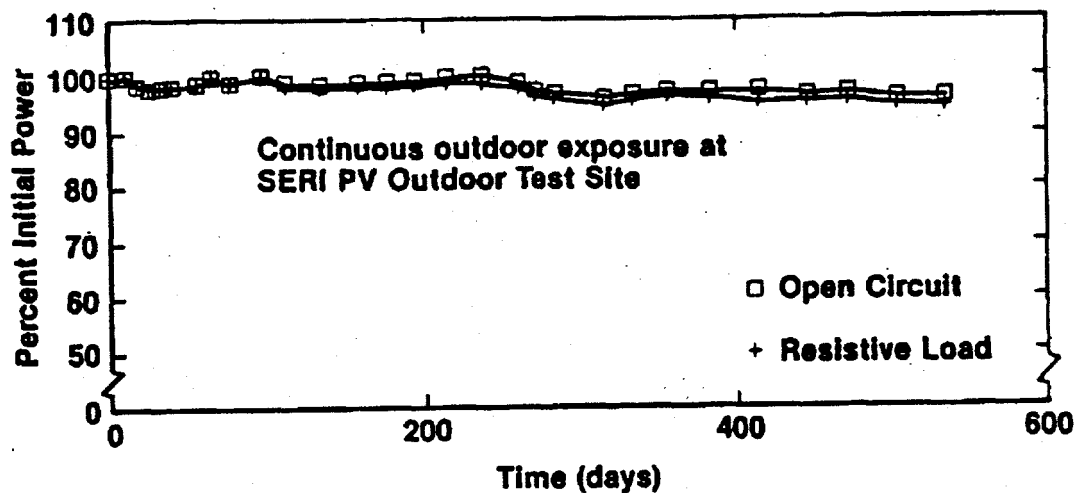


Fig. 4-4. Outdoor performance of CIS modules.

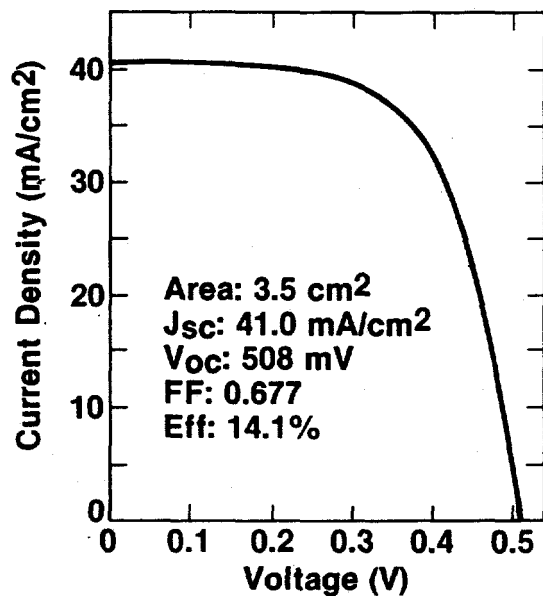
100 mW/cm² ASTM air mass 1.5 global spectrum, 25°CFig. 4-5. I-V curve for 14.1% 3.5 cm² CIS cell.

Table 4-1. Measured and predicted performance of
CuInSe₂ test device and modules.^a

	Test Device (1 cell)	Unencapsulated Modules		
		Measurements		Predictions
		0.1 m ² (55 cells)	0.4 m ² (53 cells)	0.4 m ² (53 cells)
Area ^b (cm ²)	3.5	938	3890	3900
V _{oc} /cell (mV)	508	464	464	508
J _{sc} (mA/cm ²)	41.0	39.3	37.0	41.0
V _{oc} (V)	---	25.5	24.6	26.9
I _{sc} (A)	---	0.641	2.52	2.86
Fill Factor	0.677	0.639	0.652	0.672
Eff ^b (%)	14.1	11.2	10.4	13.3
Power (W)	---	10.5	40.4	51.8

^a100 mW/cm² ASTM air mass 1.5 global spectrum, 25°C.

^bActive area for test device. Aperture area for modules.

manufacturing cost breakdown by expense category is presented in Fig. 4-6. Estimated manufacturing cost and capacity improvements are presented relative to projected costs associated with simple volume scale-up of present development and pilot level operations.

C. METALLIZATION TECHNOLOGY

1. Improvements, Benefits and Challenges

Present metallization operations represent the most significant single cost category in submodule manufacture, and offers many opportunities for dramatic cost and capacity improvements.

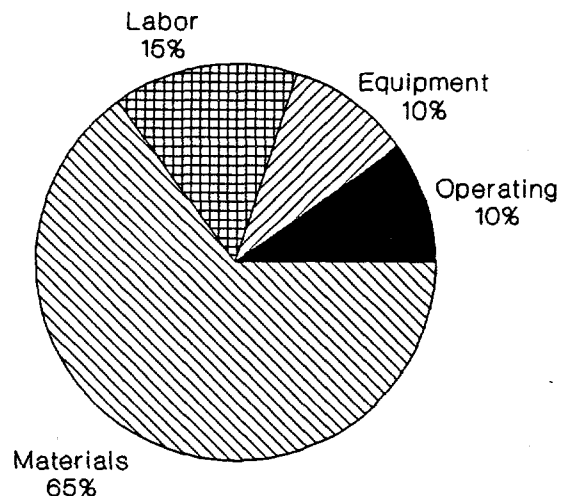


Fig. 4-6. Projected CIS manufacturing cost by expense category.

Materials costs comprise approximately three-quarters of the manufacturing costs associated with metallization. Increased materials use efficiency is achievable through alternate equipment and deposition apparatus design, proper scale-up to larger substrates, and materials reclaiming. Employing low-cost materials is possible by exploring in-house fabrication of sources from purchased raw material, exploring purity requirements for each material, alternate materials, and volume purchases. We propose to improve materials utilization by investigation of alternate deposition apparatus designs, development and installation of hardware and controls necessary for maximum substrate packing density, and scale-up of deposition technology for larger substrates. In-house source fabrication requires metallurgical studies to determine optimum source properties, design of the fabrication equipment, and development of the fabrication process itself. Metallization materials costs can be reduced 30-40%.

Equipment and labor costs can be reduced by over 50% through increased processing speeds made possible by optimization of present metallization technologies, improved equipment design, and proper scale-up to larger substrates. The tasks for increasing processing speed encompass deposition rate characterization studies, design and implementation of alternate hardware configurations for faster deposition rates and fast-cycle subsystems, and development of hardware and operational modifications for improved equipment reliability and maintainability. Improved equipment reliability and associated uptime will increase capacity and lower the associated equipment and labor costs. Specific tasks will be development of improved substrate transport, and design of monitoring hardware for maintaining proper equipment function, as well as tools for shortening equipment maintenance and set-up time. These reliability enhancements can improve the productivity of the metallization equipment and personnel by 10-15%.

Process control and resultant yield improvements are expected from development and implementation of rate and composition monitors, non-destructive diagnostics for processing defects, and appropriate particulate and organic contaminant control. Automation subtasks will be the development, design, and implementation of hardware and control schemes for unattended substrate loading, unloading, short-term storage and automatic interface from previous and to subsequent process steps, and development of process feedback diagnostics for film defects and for uniformity of film thickness and composition.

Successful implementation of materials utilization improvements, in-house source fabrication, process speed enhancements, and automation is projected to reduce the overall metallization costs by 30-40%.

2. Resources Required to Develop Improvements and Realize Benefits

The metallization development project is anticipated to require 32 months to complete. Two full-time engineers and one experienced metallization technician will be assigned to the project during this time. Project costs total approximately \$1 million, \$500,000 for labor and \$500,000 in expenses for materials, prototype equipment, and services.

We propose to work in conjunction with R&D laboratories of U.S. suppliers of deposition equipment, source materials, and thin film diagnostics, manufacturers of substrate handling and automation equipment, and private and university laboratories experienced in metallurgy, thin film diagnostics, and the scale-up issues associated with metallization processes.

D. CuInSe_2 ABSORBER TECHNOLOGY

1. Improvements, Benefits and Challenges

Processing of the CuInSe_2 absorber layer also provides many technical challenges and opportunities for module cost reduction. The projected expenses associated with the absorber layer can be reduced by over 50%.

Materials cost is presently about three-quarters of the total absorber layer processing cost. Use efficiency increases from process changes and equipment reconfiguration are expected to reduce this cost by approximately 50%. Material reclaim has the potential of increasing materials use efficiency to near 100%. Low-cost materials are achievable through in-situ synthesis of source materials from raw materials, less stringent purity specifications as appropriate, and volume purchasing. Processing strategies using alternate source materials have the potential of reducing some materials costs by as much as 95%. Absorber layer materials cost reductions of 50-80% are expected. Specific materials utilization improvement efforts will target process recipe experiments, equipment reconfiguration, material reclaim investigation, alternate source materials, and scale-up of process and equipment for larger substrates and manufacturing volumes.

Greater equipment and labor productivity are anticipated from improved control possible using diagnostics for reactive species and film composition, film adhesion, and particulate and contaminant control. Processing speed enhancements and automation of part handling and loading operations are also expected to boost throughput at essentially the same equipment and labor expense. An overall increase in productivity is expected to exceed 20%. Operating expenses and facility cost can be minimized by integrated design of multiple systems. Energy cascading and shared utilities support for sequenced operations are planned to reduce floor space

requirements as associated operating expenses by 10-25%. Specific productivity and control tasks will be development of diagnostics for reactive species measurement and control and measurement of film composition, material quality, and absorber film defects.

Successful completion of the materials utilization, productivity, and control development activities are projected to reduce the absorber layer contribution to the manufacturing cost of CIS modules by over 50%.

2. Resources Required to Develop Improvements and Realize Benefits

The absorber development project is expected to require 20 months to complete. One full-time research engineer and one experienced metallization technician will be assigned to the project along with one half-time senior engineer during this time. Project costs are \$250,000 for labor and \$150,000 in expenses for materials, prototype equipment, and services, for a total of approximately \$400,000.

We propose to work in conjunction with R&D laboratories of U.S. suppliers of deposition and annealing equipment, source materials, and thin film diagnostics, manufacturers of gas species detectors and materials reclaiming and purification equipment, and private and university laboratories experienced in solid and gas-phase chemical reaction kinetics and diagnostics, thin film measurement and characterization, and the scale-up issues associated with thin film deposition processes and equipment.

E. TRANSPARENT CONDUCTOR TECHNOLOGY

1. Improvements, Benefits and Challenges

The largest cost reduction opportunity for transparent conductor window layer deposition is in automation of the presently labor-intensive parts handling and equipment loading operations. This automation is expected to reduce labor costs by over 60% and increase mechanical yields significantly.

Increased process yield, process speed, and materials utilization is possible from improved equipment design, with an expected productivity increase of 10-30%. These include alternate source material delivery, in-situ process diagnostics for film deposition rate and quality, adhesion diagnostics, and particulate and contaminant control. Specific tasks include development of mechanized substrate handling, process diagnostics for reactive species concentrations, film deposition rate, film thickness and composition, material quality, and characterization of defects.

Implementation of these improvements is expected to reduce the cost of transparent conductor deposition by 20-30%.

2. Resources Required to Develop Improvements and Realize Benefits

The transparent conductor development project is anticipated to require 12 months to complete. One half-time research engineer and one experienced transparent conductor technician will be assigned to the project. Project costs total approximately \$120,000, comprised of \$60,000 for labor and \$60,000 in expenses for materials, prototype equipment, and services.

F. PATTERNING TECHNOLOGY

1. Improvements, Benefits and Challenges

Patterning costs are most leveraged by increased processing speed, primarily from multiple-point scribing and faster linear scribing speed. Overall rate increases can also be attained by automatic loading and part alignment. Speed increases by a factor of 2 are envisioned, lowering the overall cost of patterning by about 50%. Specific tasks are development of hardware and processes required for multi-tool operation and process development for faster linear speeds.

On-line diagnostics for effective isolation, interconnect scribe quality, laser power delivery, and mechanical scribe tip force will increase process and equipment repeatability and reliability with a resultant increase in yield. Automatic alignment, matching of coordinate systems from different machines, and electro-optical line following strategies have potential for increased active area as well as yield increases. Development efforts will focus on implementation of feedback systems for automated measurement of electrical isolation and interconnect scribe quality as well as real-time process feedback for tool pressure, tool cutting quality, and laser power delivery. Also to be developed will be pattern recognition software, imaging and optics design, feedback loop system for line following, and implementation of calibration and correlation of various coordinate systems from different equipment.

An overall patterning cost reduction of 50-60% is expected from successful completion of these tasks.

2. Resources Required to Develop Improvements and Realize Benefits

The patterning development project will last approximately 30 months. One half-time research engineer and one full-time experienced patterning technician will be assigned to the project. Project costs total approximately \$320,000, including \$220,000 for

labor and \$100,000 in expenses for materials, prototype equipment, and services.

We propose to work in conjunction with R&D laboratories of U.S. suppliers of sensors and probing systems as well as pattern recognition and CNC machining control systems. Also to be involved are private and university laboratories experienced in imaging and optics techniques as well as processing algorithms for image processing.

G. MODULE FABRICATION TECHNOLOGY

1. Improvements, Benefits and Challenges

Substantial opportunities exist to reduce costs and increase volumes of manufactured PV modules by taking a new look at how CIS submodule plates are packaged into finished PV modules.

The direct labor and materials expenses of the present CIS module fabrication process can be significantly reduced by developing alternative low-cost materials and module designs and by automating the assembly and finishing processes. Work on improving the CIS module fabrication technology will be done in close coordination with the parallel effort on improving crystalline silicon module fabrication.

Alternate module materials will be explored. Options to the prototype package that uses an EVA pottant, a glass front cover, and a polyurethane mounting frame will be evaluated.

Alternate module designs will also be explored. Since much of the module fabrication cost is relatively independent of module area, the prototype module design is driven toward larger sizes. We propose to focus our module design and module fabrication equipment efforts on modules approximately 4 ft² in size, and to evaluate options for modules 8 ft² in size.

Module fabrication labor costs will be addressed through automating the assembly and finishing processes. The first task of the automation effort will be an evaluation of conveyORIZED transport between processing machines. The second task will be to automate the soldering of electrical leads onto submodules, the "lay-up" of the submodule, pottant, and cover sheet, the lamination of the lay-up stack, and the attachment of mounting frames. The third task of the automation effort will be the automated testing of module power and high-pot resistance. Automation of module fabrication could reduce module labor costs by 50% or more.

2. Resources Required to Develop Improvements and Realize Benefits

Development of CIS module fabrication technology will be pursued as part of the work to improve the crystalline silicon module fabrication technology.

The combined module fabrication development project is expected to require 18 months to complete. Two full-time research engineers, one experienced packaging/testing technician, and one experienced product design engineer will be assigned to the project. The total project cost will be approximately \$500,000 split roughly between labor and expenses for materials, prototype equipment, and services.

H. SAFETY AND ENVIRONMENTAL TECHNOLOGY

1. Improvements, Benefits and Challenges

As technology leader, the U.S. photovoltaics industry should also lead the world in setting the standards for the safe and environmentally conscious operation of large-scale semiconductor manufacturing facilities. Improvements in equipment and facility design, increased materials use efficiency and materials reclaim, alternate feedstock materials, efficient use of utilities and water, ergonomic work station design, and waste minimization are proposed to address these expected ancillary manufacturing costs that are an inherent part of the manufacturing process. Development of appropriate strategies for waste minimization through material reclaiming or recycling, equipment design, and increased materials use efficiency will minimize the operating costs associated with waste disposal. Design of labs and processing areas to stringent standards for the prevention of health and environmental risks will increase the initial cost of operating but is expected to dramatically reduce the long-term operating costs associated with lost time from otherwise unanticipated downtime.

The project scope includes waste classification testing through outside certified laboratories, investigation of material reuse and recycling options, and development of process recipe changes and yield improvements at critical steps for minimization of waste. The project will also include investigation of alternate materials, such as low-Pb and no-Pb solder, alternate bonding techniques, and changes to the recipe or equipment at critical process steps that would reduce or eliminate potentially hazardous materials such as cadmium and hydrogen selenide.

2. Resources Required to Develop Improvements and Realize Benefits

The safety and environmental development project is anticipated to require 16 months to complete. One full-time research engineer and one half-time technician will be assigned to the project. Project costs total approximately \$250,000: \$180,000 for

labor and \$70,000 in expenses for materials and services.

We propose to work in conjunction with U.S. suppliers of solder and other raw materials and soldering/bonding equipment, and with Federal laboratories experienced in waste classification testing and materials reclaim and recycling technologies.

I. MANUFACTURING INTEGRATION TECHNOLOGY

1. Improvements, Benefits and Challenges

Automated high-density work-in-process (WIP) storage and equipment interfaces will be required to minimize the floor space, labor, and inventory cost associated with work-in-process. Ideal implementation of total manufacturing management (TMM) techniques and just-in-time (JIT) manufacturing aim at minimizing WIP, but practical considerations in manufacturing necessitate some degree of flexibility in storage of parts between machines. Early identification and implementation of the best means of accomplishing high-density parts storage with minimal handling will prove pivotal in the effective scale-up of CIS manufacturing technology. Specific project tasks will be development of high-density WIP storage equipment and automated substrate unloading, conveying, and loading interfaces between processing steps.

2. Resources Required to Develop Improvements and Realize Benefits

The manufacturing integration development project is anticipated to require 12 months to complete. One half-time research engineer and one half-time technician will be assigned to the project. Project costs are \$100,000 for labor and \$80,000 in expenses for materials, prototype equipment, and services, for a total of \$180,000.

Potential cooperative development efforts are presently being pursued with U.S. suppliers of automated material handling and control equipment, part tracking systems, and automatic storage and retrieval systems. Development activities may also require added analysis and consulting cooperation from independent engineering firms and universities experienced in the scale-up issues associated with glass and semiconductor manufacturing operations.

Document Control Page	1. SERI Report No. SERI/TP-214-4481	2. NTIS Accession No. DE92001153	3. Recipient's Accession No.
4. Title and Subtitle Research on Advanced Photovoltaic Manufacturing Technology			5. Publication Date November 1991
			6.
7. Author(s) T. Jester, C. Eberspacher			8. Performing Organization Rept. No.
9. Performing Organization Name and Address Siemens Solar Industries P. O. Box 6032 Camarillo, California 93011			10. Project/Task/Work Unit No. PV150101
			11. Contract (C) or Grant (G) No. (C) XC-1-10057-4 (G)
12. Sponsoring Organization Name and Address National Renewable Energy Laboratory 1617 Cole Blvd. Golden, Colorado 80401-3393			13. Type of Report & Period Covered Technical Report
			14.
15. Supplementary Notes NREL Technical Monitor: R. Mitchell, (303) 231-1379			
16. Abstract (Limit: 200 words) This report outlines opportunities for significantly advancing the scale and economy of high-volume manufacturing of high-efficiency photovoltaic (PV) modules. We propose to pursue a concurrent effort to advance existing crystalline silicon module manufacturing technology and to implement thin film CuInSe ₂ (CIS) module manufacturing. This combination of commercial-scale manufacturing of high-efficiency crystalline silicon modules and of pilot-scale manufacturing of low-cost thin film CIS technology will support continued, rapid growth of the U.S. PV industry.			
17. Document Analysis a. Descriptors photovoltaic modules ; thin films ; manufacturing ; crystal growth ; photovoltaics ; solar cells b. Identifiers/Open-Ended Terms c. UC Categories 270			
18. Availability Statement National Technical Information Service U.S. Department of Commerce 5285 Port Royal Road Springfield, VA 22161			19. No. of Pages 48
			20. Price A03